

	MONDAY						TUESDAY						WEDNESDAY						THURSDAY							FRIDAY						
	1	2	3	4	5	6	1	2	3	4	5	6	1	2	3	4	5	6	7	1	2	3	4	5	6	1	2	3	4	5	6	
GKK				DSP (T4) (T)	MCL (T6)		SAS (R6)					DSP (T4)	SAS (R6)						DSP (T4)				SAS (R6)	DSP (T4)	MCL (T6)					IP(T6) (T)		
UCR				MINI PROJ (PG2) (C)				NANO (PG2)		PE (T6) (T)		NANO (PG2)	PROJ (T8)		CSLII (PG2) (C)						NANO (PG2)	IOP (T8) (T)		EC W/S (E2B)					MINI PROJ (PG2) (C)			
SKA			UWBC (PG2)		MOL (T8) A BATCH (C)		UWBC (PG2)				MOL (T8) B BATCH (C)			MOL (T8) A BATCH (C)				AWP (T6) (T)			MOL (T8) B BATCH (C)			MCL (T6)		UWBC (PG2)						
HKN	EDT (PG2)	DICL (T4) A BATCH (C)					DICL (T4) B BATCH (C)				EC W/S(M2A)				EDT (PG2)		DICL (T4) A BATCH (C)				EDT (PG2)					DICL (T4) B BATCH (C)			DC(T6) (T)			
SHB	AWP (T6)				MOL (T8) A BATCH					AWP (T6)	EC W/S (M2A) (C)			MOL (T8) A BATCH		LL(T2B) A BATCH (C)								SMC (T8) (T)		EC W/S (M2A) (C)						
TAS				DSP (T4) (T)	PROJECT (T8) (C)			MINI PROJ (T6)			MSCD (T6) (T)		PROJECT (T8) (C)			MSCD (T6)				MSCD (T6)		VLSI (T6) (T)		BES (E2A) (T)	VLSI (T6)				NANO (T8) (T)			
AHM			IDS (I MCA)		MINI PROJ (T6) A BATCH (C)		BES (E2B) (T)	MINI PROJ (T6) B BATCH (C)			IDS (I MCA)		IDS (I MCA)		BES (M2B) (T)		PE (T6)			PE (T6)		IDS (I MCA)	MINI PROJ (T6) A BATCH (C)			MINI PROJ (T6) B BATCH (C)						
SHS			DICL (T4)	BMI (T8)(T)	PROJ (T8)			BES (M2A)				CS (T6) (T)	BMI (T8)		BES (M2A)					DICL (T4)		BES (M2A)(T)		LL (T2A) A BAT		DICL (T4)					BMI (T8)	
NJA			AICL (T4) B BATCH (C)			AIC (T4) (T)		AICL (T4) A BATCH (C)		AIC (T4)		CS(T6) (T)	AIC (T4)			AICL (T4) B BATCH (C)			BES (P2)(T)						AICL (T4) A BATCH (C)					EC W/S (P2)		
SAJ	BES (M2B)						BES (M2B)	RTV (T8) (T)		MOL (T8) B BATCH			IP(T6)		BES (M2B) (T)		EC W/S (M2B)		IP(T6)		MOL (T8) B BATCH	BES (M2A)(T)				EC W/S (M2A)					IP(T6) (T)	
JDB			DICL (T4)			EC W/S (E2B)			MCL (T6)			MU P (I MCA)(T)		MU P (I MCA)		MU P LAB (I MCA) (C)				MU P (I MCA)								CC (T8) (T)		MU P LAB (I MCA) (C)		
RES				BES (P2)	AIC (T4)(T)		AICL (T4)	BES (P2)						COA (T4)		AICL (T4)		BES (P2)(T)		COA (T4)		CPP (T4) LAB		BES (E2A)	AICL (T4)					COA (T4)(T)		
ANU		VLSI (T6)			AIC (T4)(T)	NANO (T8)	DICL (T4)			LL (T2B) B BATCH (C)			PROJ(T8)		VLSI (T6)		DICL (T4)		BES (P2)(T)		VLSI (T6) (T)		NANO (T8)		NANO (T8)			NANO (T8) (T)				
NIS		CN (PG2)		DC(T6)	EC W/S (E2B)		DC(T6)	DICL (T4)	RTV (T8) (T)					DC(T6)			AWP (T6) (T)		CN (PG2)			SMC (T8) (T)	CN (PG2)	MCL (T6) A BATCH			DC(T6)(T)					
PRE			RTV (T8)		MCL (T6) B BATCH (C)			MCL (T6) A BATCH (C)		RTV (T8) (T)				RTV (T8)	MU P LAB (I MCA)				RTV (T8)			MCL (T6) B BATCH (C)			MCL (T6) A BATCH (C)					MU P LAB (I MCA)		
AJI			CS (T6)	BMI (T8)(T)		BES (E2B)(T)	EC W/S (E2A)				CS (T6) (T)	CS (T6)			BES (E2B)	AICL (T4)			BES (E2B)		CS (T6)		EC W/S (E2B)			AICL (T4)						
NIZ				DES (T2A)			LL T2A A BATCH (C)		DES (T2A)		EC W/S (M2A)	DES (T2B)					EC W/S (P2)						DES (T2B)		CPP (T4) LAB		DES (T2A)		DES (T2B)			
SAN		EC W/S (M2B)			EC W/S (E2B) (C)					IOP (T8)		DEPT. DUTY			DEPT. DUTY			EC W/S (P2)				IOP (T8) (T)	EC W/S (E2B) (C)		IOP (T8)				DC(T6) (T)			

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RUB		EC W/S (M2B) (C)	DSP (T4) (T)				AICL (T4)		ADSP (T6) (T)		DEPT. DUTY		ADSP (T6)	EC W/S (M2B) (C)		ADSP (T6)						EC W/S (M2A)		COA (T4)(T)		
AMI		AICL (T4)	WC PG2			BES (E2B) (T)	WC PG2		DEPT. DUTY		WC PG2		EC W/S (P2) (C)			DEPT. DUTY			BES (E2A) (T)			WC PG2		EC W/S (P2) (C)		
ARY	CC (T8)	AICL (T4)			DEPT. DUTY		EC W/S (E2A) (C)				DEPT. DUTY		BES (M2B) (T)	CC (T8)			EC W/S (E2A) (C)		BES (E2A) (T)			CC (T8) (T)		COA (T4) (T)		
RBA		SMC (T8)			AIC (T4) (T)		SMC (T8)		DEPT. DUTY			BES (E2A)		SMC (T8)			EC W/S (E2A)		SMC (T8)(T)	BES (E2A) (T)	BES (E2A)		DICL (T4)	DEPT. DUTY		
BIJU		EC W/S (M2B)			MINI PROJ (T6)		EC W/S (E2A)							EC W/S (M2B)			EC W/S (E2A)			MINI PROJ (T6)		MINI PROJ (T6)		EC W/S (P2)		
PG2	EDT	CN	UWBC	WC	MINI PROJECT	UWCB	WC	NANO	DA		NANO	WC	EDT	CSII LAB	DA		CN	EDT	NANO	DA	WC	UWBC	CN	MINI PROJECT		
T8	CC(T)	SMC	RTV	BMI	MOC LAB/PROJECT	NANO	SMC	IOP	RTV(T)	MOC LAB/PROJECT	BMI	MOC LAB/PROJECT	RTV	SMC	CC		RTV	MOC LAB/PROJECT	IOP(T)	SMC(T)	NANO	IOP	NANO	CC	NANO(T)	BMI(T)
T6	AWP	VLSI	CS	DC	MP/MCL	DC	MP/MCL	AWP	EL II(T)	CS(T)	CS	IP(T)	DC	VLSI	EL II	AWP(T)		IP	ELII	CS	VLSI (T)	MP/MCL	VLSI	MP/MCL	DC(T)	IP
T4	CPP	DICL/AICL	DSP(T)	MATHS	AIC(T)	MATHS	DICL/AICL	AIC	HUM	DSP	AIC	HUM	MATHS	COA	DICL/AICL		DSP	MATHS	COA	HUM	CPP	DSP	DICL/AICL		CPP	COA(T)
T2A	BEE	BME	MAT	PHY	DES	DES	PHY	PHY L/LL	DES	EGS	BME	ME/EE W/S	MAT	BEE	PHY		MAT	EGS	BEE	PHY	PHY L/LL	DES	MAT	BME	ME/EE W/S	
T2B	PHY	EGS	BEE	BME	MATHS	MATHS	ME/EE W/S	PHY	PHY L/LL	DES (T2)	BEE	PHY	PHY L/LL	BME	PHY	BME	DES	DES	MAT	ME/EE W/S	BEE	PHY	DES		EGS	

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